

System Reliability Technology

Technical Report No. 6

RELIABILITY ANALYSIS OF TIMING CHANNEL CIRCUITS IN A
STATIC INVERTER

January 1966

Prepared for

Office of Reliability and Quality Assurance
National Aeronautics and Space Administration
Washington, D. C. 20546

Under Contract NASw-905

FACILITY FORM 602

N 67-19985	
(ACCESSION NUMBER)	(THRU)
46	1
(PAGES)	(CODE)
CR-82976	09
(NASA CR OR TMX OR AD NUMBER)	(CATEGORY)



This report is one of a series of technical reports issued by RTI (Research Triangle Institute), Durham, North Carolina, under NASA (National Aeronautics and Space Administration) Contract NASw-905, "Development of Reliability Methodology for Systems Engineering". The contract is administered under the direction of J. E. Condon, Director, ORQA (Office of Reliability and Quality Assurance) NASA Headquarters, Washington, D. C.

The major objective of this contract is to apply probabilistic modeling techniques developed at RTI under a previous NASA contract to a NASA in-house R and D system and to conduct research necessary to further develop techniques appropriate to probabilistic modeling. A complex 250 volt-ampere static inverter under design and development by the Astrionics Laboratory of MSFC (Marshall Space Flight Center) was selected as a representative NASA system for application and demonstration of the techniques, and the majority of the technical reports in this series are devoted to documenting results of this effort. The additional research, both basic and applied in nature, on general probabilistic modeling is documented in several specific reports also included in this series.

The effort under this contract began in April 1964 to continue for a period of approximately two years. The studies are being performed jointly in the Institute's Solid State Laboratory and Statistics Research Division under the general direction of Dr. R. M. Burger with W. S. Thompson serving as project leader.

PREFACE

This report is the sixth technical report issued under Contract NASw-905. A design reliability analysis is presented for a specific portion of the MSFC 250 volt-ampere static inverter circuit to illustrate the use of some analysis techniques for resolving design problems. Circuit performance and life were used jointly as criteria for comparing three candidate circuits and the study illustrates the importance of considering both in design considerations. Worst-case analyses utilizing simple models for circuit operation are used for performance considerations and reliability prediction models employing both two- and three-state logic for components, were used for life analyses.

Other effort under this contract consists of assembling and describing available analysis techniques and this report is intended as a reference for a sample application of elementary techniques. Major contributors in this effort were C. D. Parker and W. S. Thompson.

ACKNOWLEDGEMENT

The static inverter described in this report is being developed in the Applied Research Branch, Astrionics Laboratory, George C. Marshall Space Flight Center, NASA, Huntsville, Alabama 35812. Appreciation is extended to this group for permission to use the static inverter in this contract study.

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1.0 Introduction

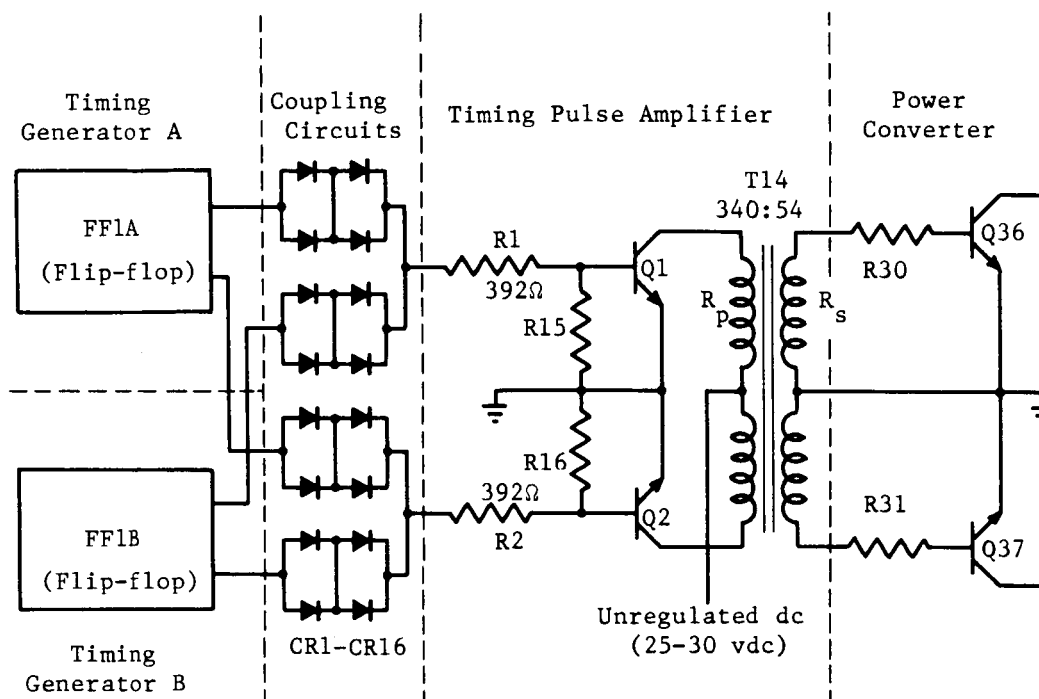
A 250 volt-ampere static inverter is being employed as a working example for the study of reliability analysis procedures. The functional operation of the inverter is described in Reference 1. A preliminary engineering design review was conducted and is presented in Reference 2. That analysis served as a first review of the circuit design and identified certain problem areas to be investigated in later studies.

This report is concerned with additional analysis of a specific portion of the inverter circuit, viz., the output circuitry of the timing section. This analysis has resulted in recommendations for modifying the design to enhance the reliability. It also serves to illustrate certain elementary reliability techniques and will be referenced in later reports.

In the following text, the design problem is first defined and the analysis approach explained. The techniques employed in the analysis are conventional consisting of both two-state and three-state logic computations for circuit life and simple worst-case type calculations for performance. It is recognized that more sophisticated techniques exist, but they, in general, require more parts data than was available for this analysis. The elementary techniques employed herein were adequate for resolving the specific questions at hand.

2.0 Problem Definition

The original version of the basic circuit analyzed is defined by the schematic diagram in Fig. 1. (The dashed boundaries identify portions of the circuit with functional circuit elements as defined in Reference 1 with element numbers conforming to designations used in the complete inverter analysis.) The circuit presented is one of five identical timing channel circuits comprising the output of the timing section of the static inverter. An additional timing channel is shown in the schematic diagram in Fig. 2 and differs from the basic circuit in that additional



$R1 = 392\Omega$ $R30 = 5\Omega$
 $R2 = 392\Omega$ $R31 = 5\Omega$
 $R15 = 1.5K$ $R_p = 19.3\Omega$
 $R16 = 1.5K$ $R_s = 0.72\Omega$

Note: Values for R_p and R_s represent average of values measured for eight transformers.

Fig. 1. Timing Channel Circuit No. 1 (Model 1)

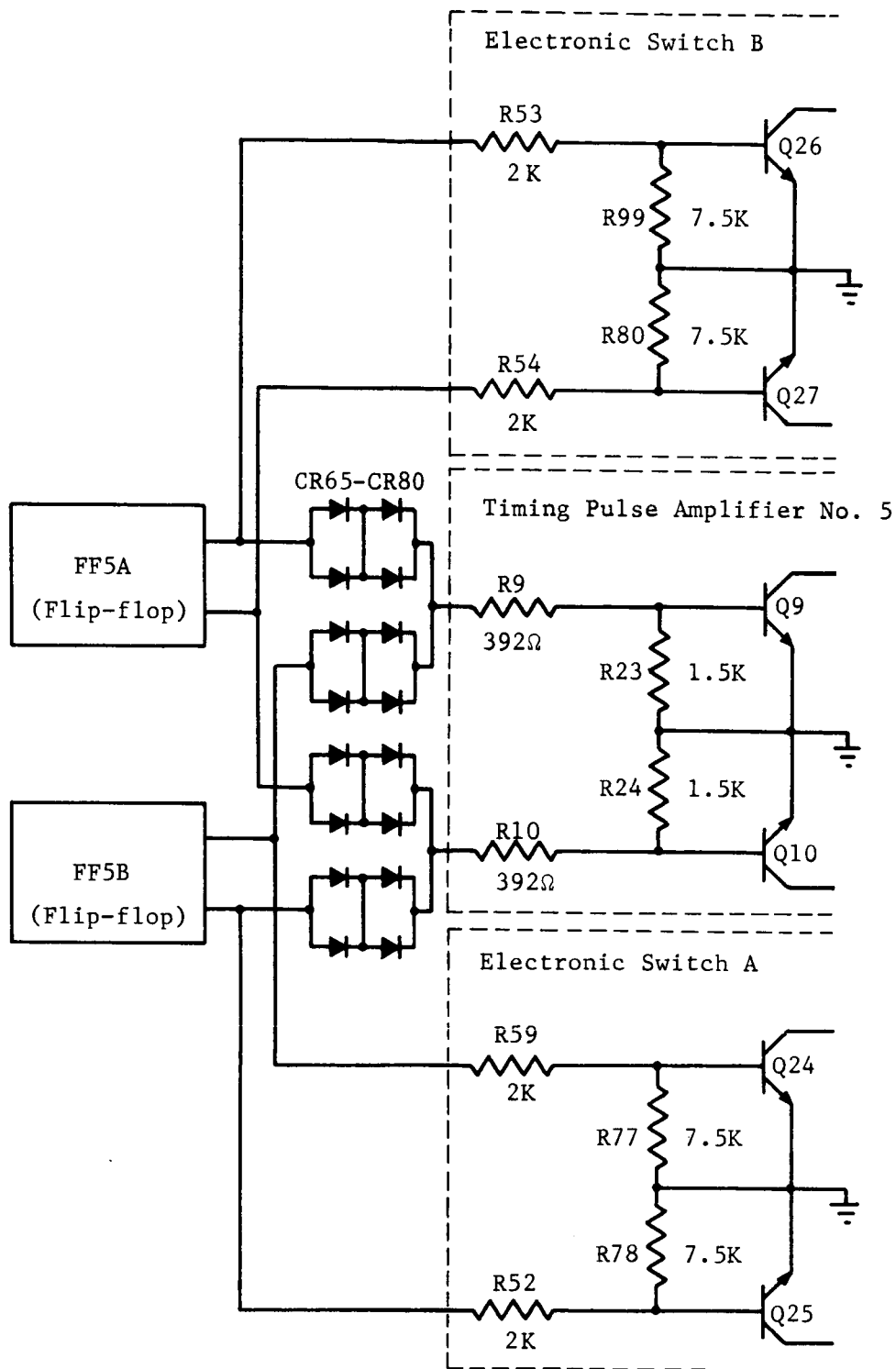


Figure 2. Timing Channel Circuit No. 5

parallel loads, the electronic switches, are on the flip-flop outputs. The results of the analysis are shown to be equally applicable to this circuit. Another similar circuit, the magnetic amplifier input driver, for which the general results are also applicable is shown in the schematic diagram in Fig. 3.

The functional operation of the circuits is described in detail in Reference 1. In summary, the major power conversion is performed in the power converters by switching transistors Q36 and Q37. There are alternately turned ON and OFF at a 400 cps rate by the timing signals which originate in either one of the two timing signal generators which operate in standby redundancy. The flip-flops in the output stage of the timing signal generators are silicon integrated circuits which do not have sufficient power capability to drive transistors Q36 and Q37 directly, hence the need for the TPA (timing pulse amplifier).

The outputs of the active flip-flop are a positive-going 400 cps square-wave pulse train and its logic complement. These provide the base drive to transistors Q1 and Q2 to alternately turn them ON and OFF. Through this push-pull operation and the transformer coupling, adequate base drive is provided to transistors Q36 and Q37.

The diodes at the interface between the redundant timing generators and the TPA serve several roles identified as follows:

- (1) The complete diode coupler element is an OR gate included primarily to isolate the active flip-flop from the inactive one.
- (2) During the high level dwell of the flip-flop output the diodes, in conjunction with R1 and R2, regulate the base currents due to their forward voltage drops.
- (3) During the low level dwell of the flip-flop output, the diodes serve as threshold devices to prevent the low level outputs from turning the transistors Q1 and Q2 during their required OFF period.

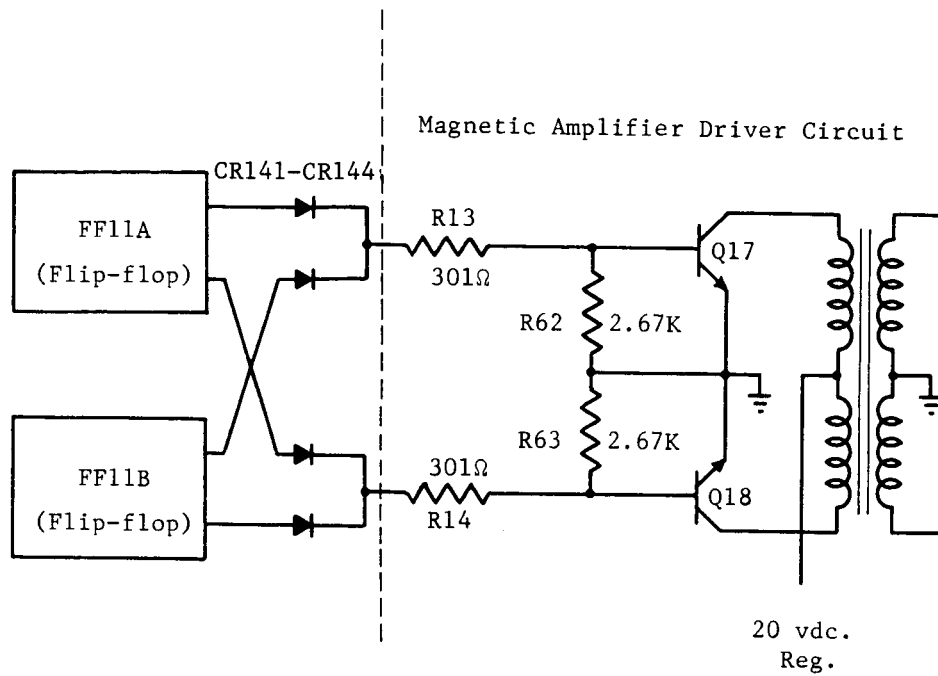


Figure 3. Magnetic Amplifier Driver Circuit

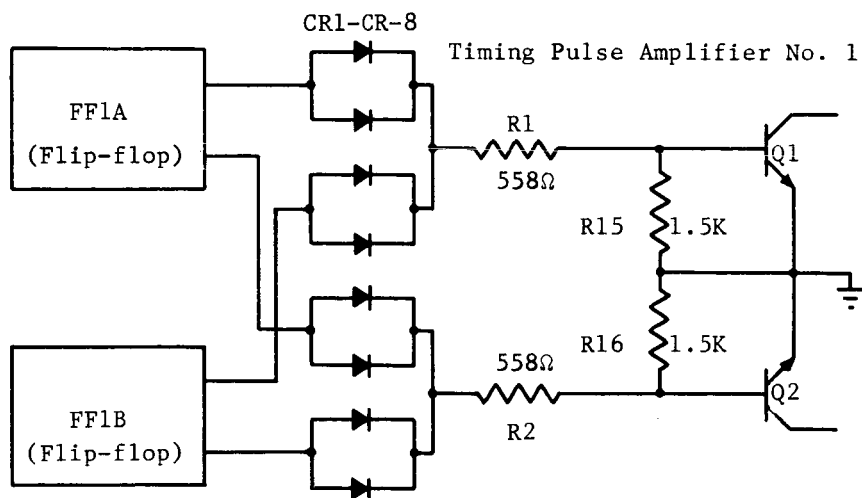


Figure 4. Timing Channel Circuit No. 1 (Model 2)

The application of these diodes and their influence on performance and life of the circuit has been a major concern in the analysis.

The problem resolved in this analysis was initially considered in Section 2.7 of Reference 2. An earlier version of this circuit used 619 ohms and the resistance values for R1 and R2, and the conclusion of that analysis was that the base currents to Q1 and Q2 were inadequate. Further study of this was considered necessary. In addition to a subsequent modification in which R1 and R2 were changed from 619 ohms to 392 ohms, this analysis considers two other circuit configurations as candidates for improving the design. The analysis is devoted to comparing the three versions of the circuit for both performance and life to select the version that offers the greatest assurance for successful operation. To facilitate discussion, the three circuit versions are explicitly defined as follows:

Model 1

Model 1 of the circuit is as shown in Fig. 1 which is the same as the original version analyzed in Ref. 2 except that R1 and R2 are 392 Ω instead of 619 Ω .

Model 2

Model 2 of the circuit is shown in Fig. 4. In this model, a pair of parallel diodes in the base circuits of transistors Q1 and Q2 are eliminated and the values of R1 and R2 are changed.

Model 3

Model 3 of the circuit which is shown in Fig. 5 eliminates the diodes and adds resistors R1' and R2'. Model 3 is the circuit recommended for use in the inverter as supported by the analyses herein.

3.0 Analyses of the Basic Timing Channel Circuit

The purpose of this section is to present in detail the considerations, assumptions, and calculations in the analysis of the three models of the basic

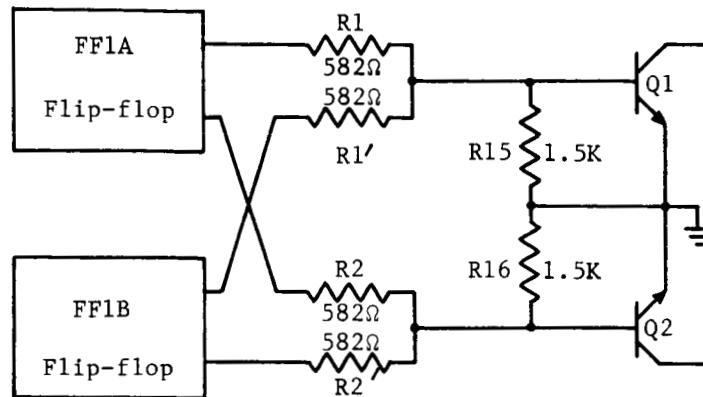


Figure 5. Timing Channel Circuit No. 1 (Model 3)

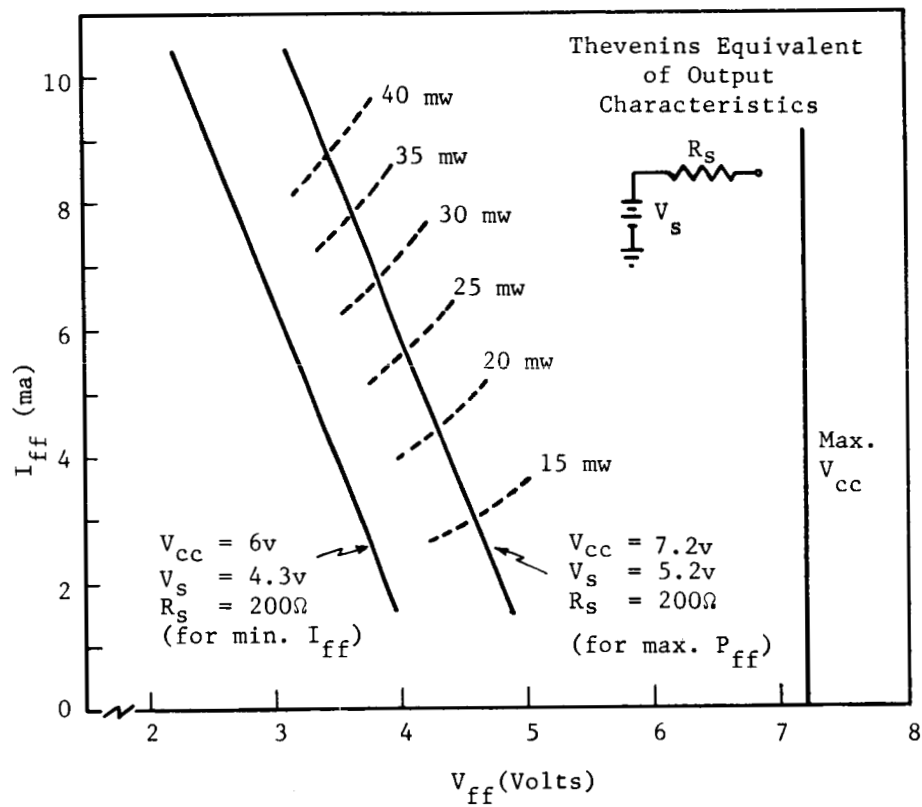


Figure 6. SN511A Emitter Follower Output Characteristics and Equivalent Circuit

timing channel circuits as defined in Section 2.0. Analyses for circuit performance are first presented in Section 3.1 and are followed by analyses for life in Section 3.2.

3.1 Analyses for Performance

Analyses for performance of all three circuit models identified in Section 2 are presented separately below. The major basis for comparing the circuits is the estimate of minimum base current to transistors Q1 and Q2 during their required ON period and the maximum power dissipation requirements of the flip-flops. These major results are summarized in Table III for comparing the models, and a concluding discussion on the comparison is presented in Section 6. Certain other aspects of the circuit related to performance are also considered below, although this is not comprehensive because many aspects of the circuit performance were discussed in Reference 2. For example, power dissipation in resistors is not discussed in this report, but in every case the dissipation is well within acceptable limits. Because the circuits are digital, worst-case type calculations are employed to compare the important performance attributes. Nominal resistor values are used in the calculations since the expected one percent variations have a negligible effect usually lost in round-off errors.

Since the application of transistors Q1 and Q2 in terms of required collector current are identical for all three circuit models, the required base drive for saturating the transistors during the ON period is first estimated from the maximum collector current requirement and the minimum dc gain, h_{FE} .

$$I_C = \frac{V_{in} - V_{CE, sat(Q1)} - \left(\frac{340}{54}\right) V_{BE(Q36)}}{R_{T9,p} + \left(\frac{340}{54}\right)^2 (R_{T9,s} + R30)} \quad (1)$$

To estimate the maximum required collector current the following worst-case conditions are assumed:

$$V_{in} = 30 \text{ v}$$

$$V_{CE,sat}(Q1) \text{ is neglected}$$

$$V_{BE}(Q36) = 1 \text{ v (manufacturer's rated value for a case temperature of } 150^{\circ}\text{C and base current of 450 ma)}$$

$$\begin{aligned} R_{T9,p} &= \text{transformer T9 primary winding resistance} \\ &= 19.3\Omega \text{ minus } 5\% (19.3\Omega \text{ represents the average measured values for eight transformers}) \end{aligned}$$

$$R30 = 5\Omega \text{ minus } 5\%$$

Using these values in (1), the maximum collector current requirements are

$$I_{C(max)} = 101 \text{ ma} . \quad (2)$$

The rated collector current of transistors Q1 and Q2 which are STC S2N2034A transistors is 3 amps allowing more than adequate safety margin. A worst-case value of h_{FE} is needed for the conditions $I_C = 101 \text{ ma}$, $V_{CE} = 1 \text{ v}$ maximum and worst-case temperature. The operating temperature range is -25°C to $+100^{\circ}\text{C}$. For the 2N2034A silicon transistor, the manufacturer claims relatively small variations of h_{FE} with temperature, and laboratory measurements on a sample of these transistors support this claim. In Reference 3, the manufacturer shows h_{FE} increasing almost linearly from 0.9 of its room temperature value at 125°C to 1.1 time its room temperature value, as the temperature is decreased to -25°C . Reference 3 also shows a negligible change in h_{FE} for collector current variations between 100 and 250 ma. These factors are considered justification for accepting the screening specification (Reference 4) value for a minimum value of h_{FE} at 125°C , 250 ma collector current, and a V_{CE} value of 1 v, i.e., 46, to be the worst-case value of h_{FE} for the application considered here.

Using the above estimate of maximum collector current requirements and minimum dc gain, the base current required to assure saturation for the assumed worst-case conditions is

$$I_{B(sat)} = \frac{101}{46} = 2.2 \text{ ma} . \quad (3)$$

The flip-flops used in the timing enerators are Texas Instruments SNS11A integrated circuits. The outputs to the TPA are derived from emitter follower configurations in the SNS11A units. The characteristic for $V_{cc} = 6 \text{ v}$ is taken directly from the manufacturer's data sheet (Reference 5) and is assumed to represent a worst-case condition for computing base-drive currents to the transistor switches. This assumes that the V_{cc} supply will always be more than 6 v. The measured output impedances from a sample of the SN511A units were much less than the 200Ω typical output impedance provided in Reference 5. The output characteristic in Figure 6 corresponding to $V_{cc} = 7.2 \text{ v}$ is assumed to represent a worst-case condition for computing flip-flop power dissipation. This characteristic was estimated by extrapolating from the manufacturer's $V_{cc} = 3 \text{ v}$ and $V_{cc} = 6 \text{ v}$ characteristics to obtain a characteristic corresponding to $V_{cc} = 7.2 \text{ volts}$. For the values of flip-flop output current expected, it is anticipated that any change in the flip-flop output impedance would be a decrease in impedance. Consequently, 200Ω is used again as a worst-case value.

The power dissipation curves for the SN511A included in Figure 6 and the calculations of flip-flop power dissipation for different outputs were determined from

$$P_{ff} = P_{(no \text{ load})} + (V_{cc} - V_{ff}) I_{ff} \quad (4)$$

where $P_{(no \text{ load})}$ = flip-flop power dissipation with no external load,

V_{cc} = supply voltage to flip-flop,

V_{ff} = emitter follower output voltage, and

I_{ff} = emitter follower output current.

This relationship assumes that the path of current flow through the flip-flop is through the emitter-follower output transistor and, consequently, the power

dissipation due to external loads is the product of the voltage drop across this path and the current through it. The no-load power dissipation term represents the losses in the remainder of the flip-flop circuit. A typical value of 7mw for $P_{(no\ load)}$ was selected from Reference 5. Since $V_{cc} > V_{ff}$ at no load, (4) is considered to provide conservative estimates.

In the following analyses, circuits Models 1, 2 and 3 are compared for two conditions defined as follows:

Condition 1: For computing minimum base currents, it is assumed that:

- (1) Flip-flop output characteristics are for $V_{cc} = 6\text{ v}$ (see Fig. 6),
- (2) p-n junction voltage drops have maximum values of 0.9 v, and
- (3) resistors exhibit nominal values.

Condition 2: For computing maximum flip-flop power dissipation, it is assumed that:

- (1) Flip-flop output characteristics are for $V_{cc} = 7.2\text{ v}$ (see Fig. 6),
- (2) p-n junction voltage drops have minimum values of 0.45 v, and
- (3) resistors exhibit nominal values.

Nominal values of resistance are assumed since their $\pm 1\%$ variations are insignificant in comparison to other variations. The junction voltage drops were selected to represent worst-case values for operation at extremes of 0°C and 100°C for ambient temperature.

Model 1

The schematic diagram for the Model 1 circuit is shown in Fig. 1. Using the Thevenin equivalent circuit shown in Fig. 6 to represent the flip-flop output characteristics, estimates of base current to transistors Q1 and Q2 are conveniently computed by

$$I_B = \frac{V_s - 2V_{CR} - V_{BE(Q1)}}{200\Omega + R1} - \frac{V_{BE(Q1)}}{R15} \quad (5)$$

Results for the two conditions are as follows:

Condition 1: $I_B = 2.1 \text{ ma}$; $P_{ff} = 12.8 \text{ mw}$.

Condition 2: $I_B = 6.3 \text{ ma}$; $P_{ff} = 28.6 \text{ mw}$.

On the basis of the assumed worst-case defined by Condition 1, base current is clearly marginal in comparison to the minimum requirement of 2.2 ma but well within flip-flop power dissipation capabilities. For Condition 2, base drive is more than adequate with flip-flop power dissipation also within requirements.

Model 2

The schematic diagram for Model 2 of the circuit is shown in Fig. 4. Since a diode drop in the base circuit has been eliminated, estimates of base current for transistors Q1 and Q2 are obtained by

$$I_B = \frac{V_s - V_{CR} - V_{BE(Q1)}}{(200\Omega + R1)} - \frac{V_{BE(Q1)}}{R15} \quad (6)$$

Equation (6) is, however, first solved for R1 and used to compute the value of R1 (and R2) that provides an acceptable design for base current. Using conservatively 2.7 ma for I_B and worst-case values of 0.9 v for $V_{BE(Q1)}$ and V_{CR} , a value of 558 Ω is obtained. With this value of R1, the results of estimates for the two conditions are:

Condition 1: $I_B = 2.7 \text{ ma}$, the design value; $P_{ff} = 14.4 \text{ mw}$.

Condition 2: $I_B = 5.4 \text{ ma}$; $P_{ff} = 25.0 \text{ mw}$.

The base drive for the worst-case represented by Condition 1 is adequate, and flip-flop power dissipation for worst-case Condition 2 is within requirements.

The Model 2 circuit definitely represents an improvement over Model 1 in performance. The elimination of a pair of parallel diodes does not jeopardize

either the isolation between redundant flip-flops or the threshold function. The motivation for considering Model 3, as a potential improvement in the circuit, is provided strictly by the attempt to remove the critical failure modes of the diodes as identified in Section 3.2.2.

Model 3

A schematic diagram of the Model 3 circuit is shown in Fig. 5. In Models 1 and 2, the diodes adequately serve to isolate the active flip-flop from the inactive one preventing loss of base drive to transistors Q1 and Q2 during the high voltage dwell of the flip-flop outputs. The occurrence of open modes of failure of the diodes on the active flip-flop output will cause circuit failure and it is shown in Section 3.2.2 that improvement in circuit life results with Model 3 if no additional critical failure modes, i.e., failure modes that cause circuit failure, are introduced. The only additional potential critical failure modes introduced are

- (1) the failure of R1, R1', R2 or R2' in a shorted mode
- (2) the failure of the inactive flip-flop in the mode with its output leads grounded, or
- (3) the shorting of the flip-flop output leads.

In considering the first failure mode, short of either resistor provides a direct path for current flow back into the output of the inactive flip-flop. The input current versus voltage characteristics, looking back into a non-failed and inactive flip-flop is of a diode threshold type for the voltage levels of interest. This was established from laboratory measurements of a number of flip-flops while connected in the actual inverter breadboard circuitry. Typically, for an applied voltage of one volt representing a maximum base-emitter voltage for Q1 and Q2 the equivalent resistance is 1.25K Ω and, of course, increases with decreasing applied voltage. In the considerations below the required value for R1, R1', R2, R2' to eliminate the criticality of the second and third failure modes identified above

is computed as a value less than $1.25K\Omega$, therefore, the short of either resistor is not critical.

It follows logically that the third failure mode is not critical if the second is not since the impedance from the higher voltage to the low voltage in the third mode is greater than the impedance to ground in the second mode. The criticality of the second mode depends on values of R_1 , R_1' , R_2 and R_2' , and the goal of the following analysis is to determine the value of these resistors such that this failure mode is not critical. With the output of the inactive flip-flop, say flip-flop 1B, grounded the base current is expressed by

$$I_B = \frac{V_s - V_{BE(Q1)}}{200\Omega + R_1} - V_{BE(Q1)} \left(\frac{1}{R_{15}} + \frac{1}{R_1} \right) . \quad (7)$$

Solving (7) for R_1 (with $R_1' = R_1$) and using the required value of 2.2 ma for base current and a worst-case condition of $V_{BE(Q1)} = 0.9$ v, the equivalent values of R_1 , R_1' , R_2 and R_2' which preclude the criticality of the failure mode are computed to be 582Ω .

Using this value of resistance, a summary of the estimates for base current and flip-flop power dissipation for several conditions are as follows:

Condition 1: With the inactive flip-flop failed such that either output lead is shorted to ground. $I_B = 2.2$ ma; $P_{ff} = 17.7$ mw.

Condition 2: With the inactive flip-flop failed so that either output lead is shorted to ground; $I_B = 5.1$ ma; $P_{ff} = 26.7$ mw.

Condition 1: For normal operation; $I_B = 3.7$ ma; $P_{ff} = 17.7$ mw.

Condition 2: For normal operation; $I_B = 5.8$ ma; $P_{ff} = 26.7$ mw.

The above results show that Model 3 is a sound choice based on performance. Even though its purpose was to eliminate a potential failure mode, the occurrence of this mode is expected to be extremely rare. For worst-case conditions, while operating in a normal non-failed mode, the base current is more than adequate and

flip-flop power dissipation is within requirements. This model of the timing channel circuit is the design recommended for use in the inverter.

It is shown in the next section that the resistive coupling technique employed in this model is also recommended for use in the magnetic amplifier driver circuit and the timing channel which drives the electronic switch; however, different values of the base resistors than those determined in this analysis are recommended.

3.2 Analysis for Life

In this analysis, the circuit is assumed to be either failed or non-failed subject to the effect of failed or non-failed states of the circuit components. Circuit failure implies that it is completely inoperative or that its performance has degraded to an extent that it no longer possesses any functional utility. The approach followed is to compare the likelihoods of survival (i.e. success or non-failure) for the three circuit models.

Because of research interest in analysis methods available for resolving problems of this type, two techniques were employed and are presented even though the results are contradictory. Both techniques are conventional but differ in depth. The first, presented in Section 3.2.1, employs simple two-state (failed versus non-failed) logic with each component failure assumed critical to circuit operation unless the failure is protected by redundancy. The second technique, presented in Section 3.2.2, uses three-state logic where each component is assumed to be in one of the three states: normal operation, failed "open", or failed "short". The basis for combining the logic events is a failure mode and effects analysis wherein the effect of each component state is considered for its effect on circuit operation. Because of the additional depth in treating component failures, more confidence is placed in the results of the second technique.

3.2.1 Analyses with Two-State Logic

Since the differences among the three models as shown in Figs. 1, 4 and 5 involve only the coupling circuits and the timing pulse amplifier, this analysis considers only the components in these circuits. The different circuit models are considered separately below.

Model 1

With the exception of parallel diodes, all components appear in logic sequence with their success probabilities combining as products. The success probabilities of identical diodes in parallel combine as $p_{CR}(2 - p_{CR})$ where p_{CR} is the success probability for a single diode. Thus, the eight pairs of parallel diodes in logic series have success probability $p_{CR}^8(2 - p_{CR})^8$. The circuit success probability $P_1(S)$ including all components of interest is

$$P_1(S) = p_{CR}^8 (2 - p_{CR})^8 p_{R1}^2 p_{R15}^2 p_{Q1}^2 \quad (8)$$

where the probabilities for identical components (e.g. R1 and R2) in the timing pulse amplifier were equated.

Model 2

Model 2 eliminates four pairs of parallel diodes, and for the remaining four pairs, the combined success probability is $p_{CR}^4(2 - p_{CR})^4$. Since the other circuit components remain unchanged, the circuit success probability for Model 2 is

$$P_2(S) = p_{CR}^4 (2 - p_{CR})^4 p_{R1}^2 p_{R15}^2 p_{Q1}^2 \quad (9)$$

To compare the success probability of Model 2 with Model 1, the ratio $P_2(S)/P_1(S)$ is considered. Assuming that the application of the resistors and transistors are nearly the same for the two models (i.e., their stresses are nearly the same), their success probabilities in the two models are considered equivalent and cancel in the ratio. An increase in the success probability of Model 2 over Model 1 thus results as represented by

$$\frac{P_2(S)}{P_1(S)} = \frac{1}{p_{CR}^4 (2 - p_{CR})^4} > 1.0 \quad (10)$$

which always holds since $0 < p_{CR} < 1$.

Model 3

In Model 3, all diodes are eliminated and resistors $R1'$ and $R2'$, identical to $R1$ and $R2$, are added. The added resistors appear in logic series with the other circuit components, thus the circuit success probability $P_3(S)$ for Model 3 is

$$P_3(S) = p_{R1}^4 p_{R15}^2 p_{Q1}^2 \quad (11)$$

To compare the success probability of Model 3 with that of Model 2, the ratio of success probabilities is again considered. Assuming again that the application of the resistors and transistors is sufficiently near the same in the two models that their success probabilities are equivalent, the ratio is

$$\frac{P_3(S)}{P_2(S)} = \frac{p_{R1}^2}{p_{CR}^4 (2 - p_{CR})^4} \quad (12)$$

To complete the comparison it is necessary to provide more information on the success probabilities p_{R1} and p_{CR} . Assuming constant failure rates λ_R and λ_{CR} for these parts, the ratio can be expressed in terms of the negative exponential life distribution of the parts, or

$$\frac{P_3(S)}{P_2(S)} = \frac{[e^{-\lambda_R t}]^2}{\left[e^{-2\lambda_{CR} t} \left(2 - e^{-\lambda_{CR} t} \right)^2 \right]^2} \quad (13)$$

The nature of this function provides that the denominator will be always greater than the numerator as $t \rightarrow 0$. The only question is the comparison at larger values of time compared to mission durations.

Typical failure rates for these type parts quoted in Reference 6 are $\lambda_R = 0.0145 \times 10^{-6}$ failure/hr. and $\lambda_{CR} = 0.001 \times 10^{-6}$ failures/hr. Using these values, it can be shown that the denominator is greater than the numerator for all

$t > 0$. Thus $P_2 > P_3$, or assuming that the quoted failure rates are realistic in terms of their relative values, Model 2 is concluded to be superior to Model 3 in terms of success probabilities using two-state logic.

It is emphasized here that this same result is not obtained in Section 3.2.2 using the three-state logic as supported by a failure mode and effects analysis. This serves to illustrate pitfalls that may result at times from using over-simplified models. It is also noted that the above result is not general. For example, at some value of $\lambda_{CR} > \lambda_R$ the results reverse.

Comparing Model 3 with Model 1, the ratio is

$$\frac{P_3(S)}{P_1(S)} = \frac{P_{R1}^2}{P_{CR}^8 (2 - P_{CR})^8} \quad (14)$$

Again, assuming the negative exponential life distribution and the failure rates quoted above for the resistor and diode, it can be shown by similar argument that $P_1 > P_3$. Again, the result differs from that obtained in Section 3.2.2 using three-state logic.

3.2.2 Analyses with Three-State Logic

Using three-state logic to compute the probability of circuit survival provides added sophistication over the analyses using two-state logic in Section 3.2.1. In this analysis, the interest is on the state of the circuit component between each pair of terminals. The component is assumed to be in one of the three operating modes of (1) normal ("non-failed" or "success") operation, (2) failed "open", or (3) failed "short". For each circuit model, a failure mode and effects analysis is first performed wherein the possible failure modes of each circuit component are identified and the effect it has on circuit operation established. Using three-state logic, an expression for the probability of survival is derived as a basis for comparing the three models from the standpoint of life.

To simplify the analysis, the problem is formulated in the simplest manner that is adequate to resolve the questions at hand. Referring to Figs. 1, 4 and 5 for

the three circuit models, the analysis is approached on the basis whereby given that one or the other of the flip-flops is active, the interest is on the probability that the circuit does not fail due to failure of any other part. This immediately eliminates the event whereby both flip-flops may be active or both may be inactive, either of these obviously causing failure of the timing channel. As will be demonstrated in the analyses, the inactive flip-flop is treated simply as a passive three terminal impedance device in consideration of failure modes.

Analyses for each of the circuit models are presented separately below.

Model 1

Model 1 of the timing channel circuit is presented in Figure 1. To simplify the logic, an abbreviated version of the circuit is presented in Figure 7 which is applicable also to Model 2.

The failure mode and effects analysis of the circuit in Figure 7 is summarized in Table I which contains a listing of the failure modes of each circuit component between its terminal pairs and the resulting effect on circuit operation. The referenced notes are presented in Section 4.

To derive the probability of circuit survival, the following logic notation is introduced. For the element denoted by X, let

x = event of normal operation (i.e., no failure),

X = event of failure (either open or short),

X_o = event of failing open, and

X_s = event of failing short.

Also, let a bar over a letter denote the complement of an event such that

\bar{X} = event that X does not occur.

By the above definition, it also follows that $x = \bar{X}$

The appropriate failure events to be included in the derivation of the success probability are tabulated in Table I. If in the failure mode and effects analysis,

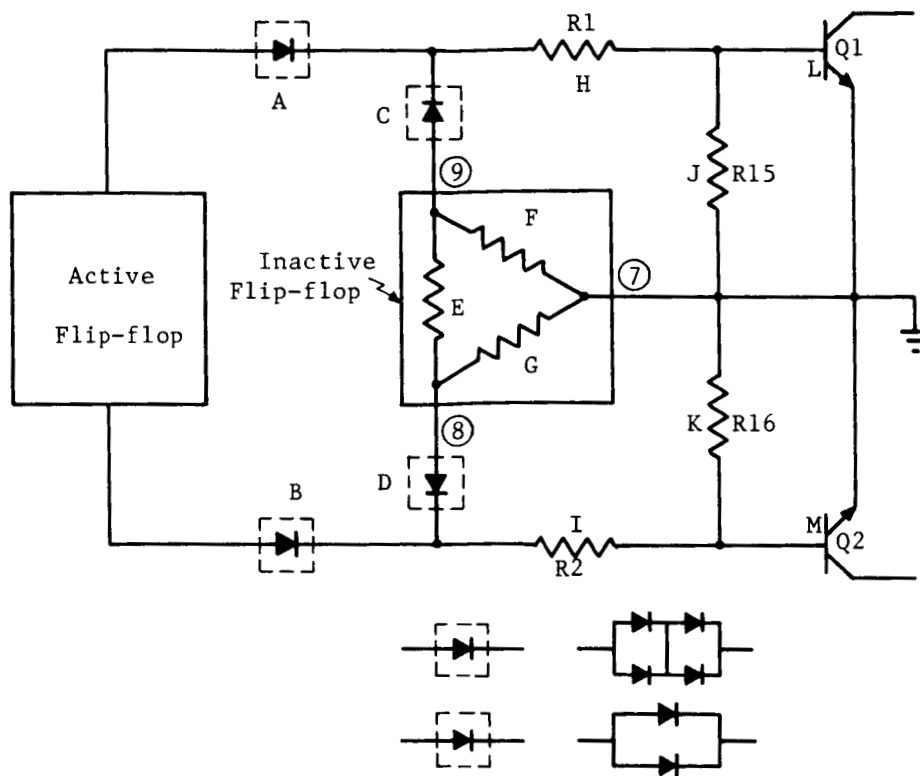


Figure 7. Basic Circuit Configuration for Performing Failure Mode and Effects Analysis for Models 1 and 2

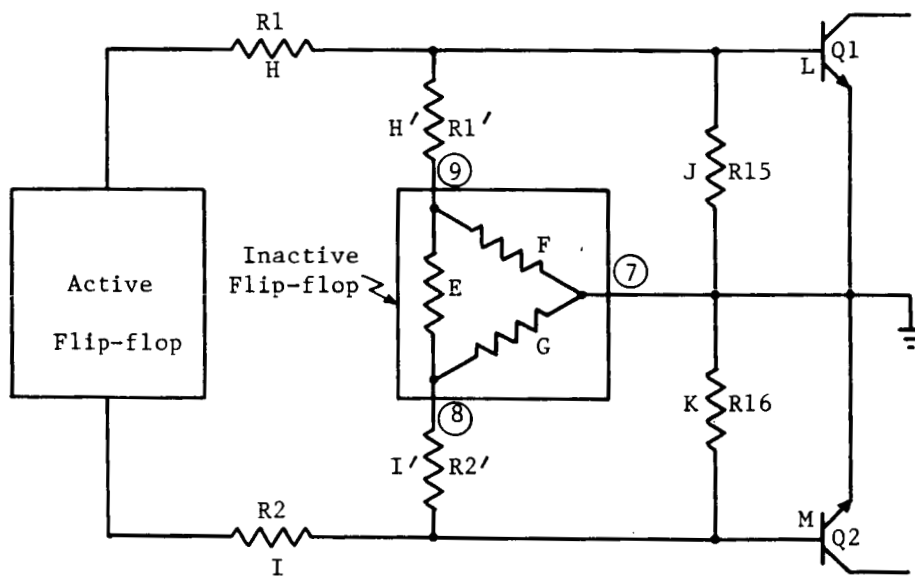


Figure 8. Basic Circuit Configuration for Performing a Failure Mode and Effects Analysis for Model 3

the failure of an element does not cause circuit failure, i.e., is not a critical failure mode, it is not included in the derivation. The event of circuit success is synonymous with the event that critical failures, either singly or in combination, do not occur. In a probability statement, this is expressed by

$$P'_1(S) = P(\overline{A_O + B_O + C_S + D_S + H + I + J_S + K_S + L + M}) \quad (15)$$

where "+" denotes the union of events. Since

$$P(\overline{X + Y}) = P(\overline{X}, \overline{Y}) \quad (16)$$

with the comma denoting intersection,

$$\begin{aligned} P'_1(S) &= P(\overline{A_O}, \overline{B_O}, \overline{C_S}, \overline{D_S}, \overline{H}, \overline{I}, \overline{J_S}, \overline{K_S}, \overline{L}, \overline{M}) \\ &= P(\overline{A_O}, \overline{B_O}, \overline{C_S}, \overline{D_S}, h, i, \overline{J_S}, \overline{K_S}, \ell, m) . \end{aligned} \quad (17)$$

Assuming the failures are statistically independent and equating the probabilities of identical parts,

$$P'_1(S) = \left[P(\overline{A_O})P(\overline{C_S})P(h)P(\overline{J_S})P(\ell) \right]^2 . \quad (18)$$

Now element A is a diode-quad configuration with a shunting connection or two series pairs of parallel diodes. For a single pair of parallel diodes, the probability of both not failing open is $p_o(2 - p_o)$ where p_o represents the probability of a single diode not failing open. Thus for the diode-quad

$$P(\overline{A_O}) = p_o^2(2 - p_o)^2 . \quad (19)$$

Element C is also an identical diode-quad configuraton; however, in this case, the failure mode of interest is a short. For a single pair of parallel diodes, the probability of neither failing short is p_s^2 where p_s represents the probability of a single diode not failing in the shorted mode. For the diode-quad, the event of interest is that both parallel pairs of diodes not fail in the shorted mode simultaneously with the probability expressed by

$$P(\overline{C_S}) = p_s^2(2 - p_s^2) \quad (20)$$

Table I. Tabulation of Part Failure Modes and Effects for Models 1 and 2

(Reference: Figure 7)

<u>Part</u>	<u>Failure Mode</u> <u>(Short or Open)</u>	<u>Effect on</u> <u>Timing Channel</u>	<u>Failure</u> <u>Event</u>	<u>Notes</u> (Ref.: Sec. 4)
Diode Config. A	Short	Sustained Operation	- -	1
	Open	Failure	A _O	1
Diode Config. B	Short	Sustained Operation	- -	1
	Open	Failure	B _O	1
Diode Config. C	Short	Failure	C _S	2
	Open	Sustained Operation	- -	2
Diode Config. D	Short	Failure	D _S	2
	Open	Sustained Operation	- -	2
Inactive Flip-Flop:				
⑨ to ⑦	Both	Sustained Operation	- -	3
⑧ to ⑦	"	" "	- -	3
⑨ to ⑧	"	" "	- -	3
R1	Both	Failure	H	4
R2	Both	Failure	I	4
R15	Short	Failure	J _S	5
	Open	Sustained Operation	- -	5
R16	Short	Failure	K _S	5
	Open	Sustained Operation	- -	5
Q1:				
Coll. to Base	Both	Failure	{ L }	6
Base to Emit.	Both	"		
Coll. to Emit.	Both	"		
Q2:				
Coll. to Base	Both	Failure	{ M }	6
Base to Emit.	Both	"		
Coll. to Emit.	Both	"		

Substituting (19) and (20) into (18), the success probability for Model 1 is

$$P_1'(S) = \left[p_o^2 (2 - p_o)^2 p_s^2 (2 - p_s^2) P(h) P(\bar{J}_s) P(\ell) \right]^2 \quad (21)$$

This expression will be used for comparison with Models 2 and 3 below.

Model 2

Model 2 of the circuit is shown in Figure 4, however, the simplified version presented in Figure 10 is used for this analysis. The circuit configuration for Model 2 is identical to that of Model 1 except for the elimination of a parallel pair of diodes. Since the functions performed by the remaining diodes are adequate and identical to the diode-quads, the failure mode and effects analysis in Table I and the derivation of the circuit success probability through (18) is identical to that of Model 1. For Element A

$$P(\bar{A}_o) = p_o (2 - p_o) , \quad (22)$$

and for Element C

$$P(\bar{C}_s) = p_s^2 . \quad (23)$$

Substitution of (22) and (23) into (18) yields for the success probability of Model 2

$$P_2'(S) = \left[p_o (2 - p_o) p_s^2 P(h) P(\bar{J}_s) P(\ell) \right]^2 . \quad (24)$$

As in Section 3.2.1, the ratio of success probabilities is used to compare models, thus

$$\frac{P_2'(S)}{P_1'(S)} = \frac{1}{p_o^2 (2 - p_o)^2 (2 - p_s^2)^2} \quad (25)$$

where the similar terms in the numerator and denominator are assumed equal and thus cancel.

The result depends on whether the denominator is greater than or less than unity. It can be shown without great difficulty that near $p_o = p_s = 1$, the

denominator is greater than unity.

Letting $q_o = 1 - p_o$ and $q_s = 1 - p_s$, the denominator of (25) can be written as

$$\text{Denominator (D)} = (1 - q_o^2)^2 (1 + 2q_s - q_s^2)^2. \quad (26)$$

For q_o and q_s near zero, terms of second degree and higher can be neglected. Hence,

$$D \approx 1 + 4q_s > 1,$$

and it follows that

$$P'_1(S) > P'_2(S)$$

subject to the assumption that q_o and q_s are very near zero.

Model 3

Model 3 of the circuit is shown in Figure 5, however, for the purpose of performing the failure mode and effects analysis, a simplified version is shown in Figure 8. The analysis is summarized in Table II. Using the failure events tabulated therein, the success probability is expressed as

$$\begin{aligned} P'_3(S) &= P(\overline{H} + \overline{I} + \overline{J}_s + \overline{K}_s + \overline{L} + \overline{M}) \\ &= P(\overline{H}, \overline{I}, \overline{J}_s, \overline{K}_s, \overline{L}, \overline{M}), \end{aligned} \quad (27)$$

Using the same simplifying assumptions as in the analysis of Model 1, this reduces to

$$P'_3(S) = \left[P(h) P(\overline{J}_s) P(\overline{l}) \right]^2. \quad (28)$$

Again using the ratio of success probabilities for comparison of models

$$\frac{P'_3(S)}{P'_2(S)} = \frac{1}{p_o^2 (2 - p_o)^2 p_s^2} > 1.0, \quad (29)$$

since p_o and p_s are less than unity. Thus, $P_3 > P_2$ showing that Model 3 is superior to Model 2 on the basis of success probabilities obtained with three-state logic. This is in direct contrast to the result obtained in Section 3.2.1 using two-state logic and illustrates the advantage of using the added sophistication.

Table II. Tabulation of Part Failure Modes and Effects for Model 3

(Reference: Figure 8)

<u>Part</u>	<u>Failure Mode (Short or Open)</u>	<u>Effect on Timing Channel</u>	<u>Failure Event</u>	<u>Notes</u> (Ref.: Sec. 4)
Inactive Flip-Flop				
⑨ to ⑦	Both	Sustained Operation		7
⑧ to ⑦	Both	Sustained Operation		7
⑨ to ⑧	Both	Sustained Operation		7
R1	Both	Failure	H	8
R2	Both	Failure	I	8
R1'	Both	Sustained Operation		9
R2'	Both	Sustained Operation		9
R15	Short	Failure	J _s	10
	Open	Sustained Operation		
R16	Short	Failure	K _s	10
	Open	Sustained Operation		
Q1:				
Coll. to Base	Both	Failure	{ L }	11
Base to Emit.	Both	"		
Coll. to Emit.	Both	"		
Q2:				
Coll. to Base	Both	Failure	{ M }	11
Base to Emit.	Both	"		
Coll. to Emit.	Both	"		

The additional advantage gained by Model 2 over Model 3 resulted from elimination of the diodes and their critical modes of failure without introducing critical failure modes of the remaining elements or the added elements R1' and R2'.

Comparing Model 3 with Model 1,

$$\frac{P'_3(S)}{P'_1(S)} = \frac{1}{p_o^4 (2 - p_o)^4 p_s^4 (2 - p_s^2)^2} > 1.0. \quad (30)$$

Since $P'_3 > P'_1 > P'_2$, Model 3 is selected as the superior circuit and is the model recommended for use in the inverter with further supporting analyses presented in Section 3.1.

4.0 Notes Accompanying Failure Mode and Effects Analyses

A failure mode and effects analysis of the basic timing channel circuit was performed in Section 3.2.2 and summarized in Tables I and II. The notes referenced in those tables are presented below and provide the justification for designating or rejecting a part failure as critical.

(1) A short of either diode configurations A or B as defined in Figure 7 still maintains a continuity of the drive to the timing pulse amplifier. The transistor base current will be excessive but not detrimental either from the point-of-view of transistor power dissipation or transistor switching transients nor will the power capabilities of the flip-flop be exceeded. The shorted mode of failure is thus not considered critical.

(2) An open of either diode configuration C or D obviously does not cause circuit failure since the violation between flip-flops is maintained. However, in the event of a short circuit, failure does occur. As described in Section 3.1 under Model 3, the input current versus voltage characteristics, looking back into a non-failed and inactive flip-flop to ground, exhibits a diode threshold type characteristic. With either diode configuration shorted, the applied voltage during the high level voltage dwell of the active flip-flop is sufficiently great

to cause significant conduction through the inactive flip-flop. This subtracts from the transistor base current resulting in less than the required minimum of 2.2 ma.

(3) Neither a short nor open between any of the three terminals of the inactive flip-flop as illustrated in Figure 7 result in circuit failure. In the case of short, the diodes between the base drive circuit and the inactive flip-flop are reverse biased providing adequate isolation between the drive circuits and from either drive circuit to ground. An open failure obviously has insignificant effect on circuit operation.

(4) Both open and short modes of failure of R1 and R2 are assumed to be critical. The open mode simply results in loss of drive to the timing pulse amplifier. In the short mode continuity for drive to the timing pulse amplifier is still maintained. The circuit would be expected to continue operating for a brief period; however, the loss of base current regulation will cause excess power dissipation in the flip-flops causing it to eventually fail. When the redundant timing channel resumes the drive, it too, will fail for the same reason.

(5) Resistors R15 and R16 are provided primarily as paths for transistor collector base leakage currents I_{CBO} during the required OFF period. In the event a short of either resistor occurs, the base of the transistor is grounded resulting in circuit failure. If an open mode of failure occurs, their primary function will be jeopardized; however, is not considered to result in circuit failure. The maximum collector-emitter voltage during this period is 60 vdc. Manufacturer's rating states a maximum value of 0.75 ma for leakage current for the condition of 150°C ambient temperature and a collector-emitter voltage of 80 v. Values measured with samples all exhibited leakage currents of less than 10 μ a at 30 v collector-emitter voltage and 100°C ambient temperature. Temperature is known to be the more critical environment with I_{CBO} increasing with increasing temperature. With such small values of I_{CBO} , the conduction of the transistor would be negligible

during the required OFF period, hence, not causing circuit failure. The inverter breadboard circuit has been operated for extended periods of time without difficulty in ambient temperature extremes of 0°C and 100°C with R15 and R16 open circuited.

(6) Transistors Q1 and Q2 failing by either opening or shorting between any pair of the three terminals will obviously cause circuit failure.

(7) The inactive flip-flop in the Model 3 application still does not cause circuit failure for any of the three failure modes shown. Justification was presented in Section 3.1 wherein the circuit was designed for the value of R1, R1', R2' and R2' that prevented potential criticality.

(8) The discussion in Note 4 applies directly.

(9) Neither an open or short of R1' or R2' cause failure. The open mode obviously has an insignificant effect. The justification for eliminating the shorted mode as critical is given in the analysis of Section 3.1.

(10) The discussion in Note 5 applies directly.

(11) The discussion in Note 6 applies directly.

5.0 Consideration of Similar Circuits

The previous section was concerned with the analysis and redesign of the basic timing channel circuit which accounts for five of the circuits in the static inverter. Two similar circuits for which the analyses and results are applicable are timing channel circuit No. 5 shown in Figure 2 and the magnetic amplifier driver circuit shown in Figure 3. The analyses of these circuits, presented below are not as detailed as for the basic circuit in Section 3.0. Rather, the performance and life are discussed collectively for the various versions of the circuit considered relying on the previous results.

5.1 Timing Channel Circuit No. 5

As shown in Figure 2, the original version of the timing channel circuit No. 5 is the same as the basic circuit for the other five channels except for the additional load on the flip-flop provided by the electronic switches. This added load increases the power dissipation requirements on the flip-flops and is important in considering modifications of the circuit such as in Model 3 of the basic circuit.

For the circuit as shown in Figure 2, estimates of base current for transistor Q1 and Q2 and flip-flop power dissipation are computed in a manner similar to that in Section 3.1. The worst-case conditions defined in Section 3.1 as Conditions 1 and 2 are again used with the following exceptions. In computing the minimum base currents for transistor Q9, it is assumed that the base-emitter voltage drop of transistor Q26 will not vary more than 0.1 v from the assumed worst-case base-emitter voltage drop for transistor Q9 due to their strong correlation through their mutual temperature dependence. However, for computing maximum flip-flop power dissipation, the drops are assumed equal at a worst-case value of 0.45 v.

For Model 1 of the circuit, estimates for the two worst-case conditions are:

Condition 1: With $V_{BE(Q26)} = 0.8 \text{ v.}$; $I_B = 1.7 \text{ ma}$, $P_{ff} = 15.7 \text{ mw}$.

Condition 2: With $V_{BE(Q26)} = 0.45 \text{ v.}$; $I_B = 5.6 \text{ ma}$, $P_{ff} = 33.2 \text{ mw}$.

Even though flip-flop power dissipation is within its rating with the added load, the base current is less than the required minimum of 2.2 ma stated in (3) and is thus inadequate.

For the Model 2 version of this circuit, the resistance value of 523Ω for R9 and R10 are specified to conservatively provide 2.5 ma of base current to transistors Q9 and Q10. The results for worst-case conditions with Model 2 are:

Condition 1: With $V_{BE(Q26)} = 0.8 \text{ v.}$; $I_B = 2.5 \text{ ma}$, $P_{ff} = 18.0 \text{ mw}$.

Condition 2: With $V_{BE(Q26)} = 0.45 \text{ v.}$; $I_B = 5.2 \text{ ma}$, $P_{ff} = 31.6 \text{ mw}$.

Model 2 of this circuit is thus adequate in performance.

An adequate design can also be achieved with the Model 3 version using resistive coupling. Considering again that failure with the inactive flip-flop output leads shorting to ground is the potential critical failure mode of major concern, the value of R_9 , R_9' , R_{10} and R_{10}' which assures the minimum required base current of 2.2 ma is computed to be 476Ω . A summary of results for worst-case conditions for Model 3 with resistive coupling is as follows:

Condition 1: With the inactive flip-flop failed with either output lead shorted to ground and $V_{BE(Q26)} = 0.8 \text{ v.}$; $I_{B(Q1)} = 2.2 \text{ ma}$, the design value; $P_{ff} = 23.4 \text{ mw}$.

Condition 2: With the inactive flip-flop failed with either output lead shorted to ground and $V_{BE(Q26)} = 0.45 \text{ v.}$; $I_{B(Q1)} = 5.3 \text{ ma}$, $P_{ff} = 36.4 \text{ mw}$.

Condition 1: For normal operation, $V_{BE(Q1)} = 0.9 \text{ v}$ and $V_{BE(Q26)} = 0.8 \text{ v.}$; $I_{B(Q1)} = 4.1 \text{ ma}$, $P_{ff} = 23.4$.

Condition 2: For normal operation and $V_{BE(Q26)} = 0.45 \text{ v.}$; $I_{B(Q1)} = 6.3 \text{ ma}$, $P_{ff} = 36.4 \text{ mw}$.

Based on the above results, the circuit is adequate in performance.

In the considerations for circuit life, the results of the analysis in Section 3.2 are directly applicable. On the basis of circuit success probability calculations employing two state logic, the added components provided by the electronic switch merely appear as additional logic elements in series with those of the basic circuit configuration. Thus in performing the ratio comparisons of success probabilities, these additional product terms will merely cancel.

Using three-state logic failure mode and effects considerations reveal that additional critical failure modes are present but in comparing the circuits, do not affect the result. With FF5A in Figure 2 active, for example, an open mode of failure for either R_{52} or R_{53} will cause immediate switching to the redundant timing generator, and if it is operative, result only in a transient in the drive

to the timing pulse amplifier. A shorted mode of failure for either of these resistors will cause excess drive to the appropriate transistor in the electronic switch causing overheating and eventual failure at which time operation will switch to the opposite channel. This situation will occur in all three versions of the circuit. The logic events are in series with the component success probabilities and will cancel in the ratio comparisons of the circuit success probabilities revealing the same result as in Section 3.1.2 that the circuit with resistive coupling is superior.

5.2 Magnetic Amplifier Driver Circuit

The schematic diagram for the magnetic amplifier circuit is shown in Figure 3. This circuit is identical to the basic timing channel circuit in configuration and operation, however, it utilizes different transistors and operates at 4800 cps.

The performance analysis is conducted in a manner similar to that in Section 3.1. Transistors Q17 and Q18 are type S2N2102. Maximum collector current requirements are computed to be 102 ma. The dc gain of transistor Q1 and Q2 is not specified in manufacturer's data for the conditions corresponding to this application, however, by linear extrapolation from the nearest specified conditions, a minimum value for h_{FE} of 35 is established for the maximum collector current and a temperature of 0°C. The minimum required base current is thus 2.9 ma.

The worst-case conditions defined in Section 4.1, Condition 1 and 2, are again used in the analyses. A version of the circuit analogous to Model 1 of the other circuits was not considered. For the Model 2 version as shown in Figure 3, estimates of transistor base current and flip-flop power dissipation for worst-case conditions are presented below.

Condition 1: $I_B = 4.7 \text{ ma}$; $P_{ff} = 20.0 \text{ mw}$.

Condition 2: $I_B = 8.4 \text{ ma}$; $P_{ff} = 38.8 \text{ mw}$.

On the basis of transistor base current, the design is clearly adequate to provide the required minimum of 2.9 ma. Maximum flip-flop power dissipation is greater than any computed previously. Whether this is to be considered excessive is subject to question since the derating characteristics of the SN511A flip-flop are not specified by the manufacturer. Power dissipation could be decreased by redesigning for resistance values of R13 and R14 to provide less but adequate transistor base current, however, this was not performed since the Model 3 version is the preferred circuit.

In considering the Model 3 version using resistive coupling, the goal is again to design to remove the possible critical failure mode of the inactive flip-flop output leads shorting to ground. Using 3 ma as the design value for base current, a value of 412Ω for R13, R13', R14 and R14' is established. A summary of estimated base currents and flip-flop power dissipation for conditions of interest are as follows:

Condition 1: With the inactive flip-flop failed with either output lead shorted to ground; $I_B = 3.0$ ma, the design value;
 $P_{ff} = 22.3$ mw.

Condition 2: With the inactive flip-flop failed with either output lead shorted to ground; $I_B = 6.5$ ma, $P_{ff} = 34.4$ mw.

Condition 1: For Normal operation; $I_B = 5.2$ ma, $P_{ff} = 22.3$ mw.

Condition 2: For Normal operation; $I_B = 7.6$ ma, $P_{ff} = 34.4$ mw.

On the basis of the above results, the circuit employing resistive coupling is adequate in performance.

Since the circuit configuration is identical to the basic timing circuit, analyses for life provide the same results as obtained in Section 3.2, i.e., on the basis of circuit life, the circuit employing resistive coupling is superior.

6.0 Summary of Analyses and Conclusions

Three models of the basic timing channel circuit for comparison were defined in Section 2 and are shown in Figure 1, 4 and 5. Two similar circuits, timing channel circuit No. 5 and the magnetic amplifier driver circuit, also affected by the analysis are shown in Figures 2 and 3. Detailed analyses of the basic circuit from the points-of-view of both performance and life are presented in Section 3 and the results extrapolated to the similar circuits in Section 5.

The major bases for comparing the circuit models in performance were the minimum base currents to the switching transistors (e.g., Q1 and Q2 in Figure 1) in the push-pull amplifier stage and the maximum power dissipation of the flip-flops providing the base currents. For circuit life, the comparisons are made on the basis of success probabilities or likelihoods of survival using both two-state (success vs. failure) logic and three-state (short, open, normal) logic for circuit components.

The results of performance analyses are summarized for comparison in Table III. The minimum required base currents for saturating the switching transistors during their required ON period were estimated in Section 3.1 from maximum collector current requirements and minimum values of transistor dc gain. The minimum base currents for each model are associated with Condition 1 in Table III, and the maximum power dissipation with Condition 2. Condition 1 represents a worst-case situation in which the supply voltage to the flip-flops is a minimum, the output impedance of the flip-flops is at a maximum, and the p-n voltage drops in the circuit are at their extreme value which minimizes the base current. Condition 2 represents a worst-case situation in which the supply voltage to the flip-flops is a maximum, the output impedance of the flip-flops is at a maximum, and the p-n voltage drops in the circuit are at their extreme value which maximizes the flip-flop output current and power dissipation. Resistor variations were neglected since the effect of their $\pm 1\%$ variations was determined to be insignificant.

Table III. Summary of Results of Performance Analyses

Circuit	Performance Characteristic	Model 1		Model 2		Model 3			
		Condition		Condition		Normal Operation		With Flip-flop Failure	
		1	2	1	2	1	2	1	2
Basic Timing Channel Circuit	Q1, Q2 Base Current(ma) (Min. Required 2.2 ma)	2.1	6.3	2.7	5.4	3.7	5.8	2.2	5.1
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 25°C)	12.8	28.6	14.4	25.0	17.7	26.7	17.7	26.7
Timing Channel Circuit No. 5	Q9, Q10 Base Current(ma) (Min. Required: 2.2 ma)	1.7	5.6	2.5	5.2	4.1	6.3	2.2	5.3
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 25°C)	15.7	33.2	18.0	31.6	23.4	36.4	23.4	36.4
Magnetic Amplifier Driver Circuit	Q17, Q18 Base Current(ma) (Min. Required: 2.9 ma)	---	---	4.7	8.4	5.2	7.6	3.0	6.5
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 250°C)	---	---	20.0	38.8	22.3	34.4	22.3	34.4

6.0 Summary of Analyses and Conclusions

Three models of the basic timing channel circuit for comparison were defined in Section 2 and are shown in Figure 1, 4 and 5. Two similar circuits, timing channel circuit No. 5 and the magnetic amplifier driver circuit, also affected by the analysis are shown in Figures 2 and 3. Detailed analyses of the basic circuit from the points-of-view of both performance and life are presented in Section 3 and the results extrapolated to the similar circuits in Section 5.

The major bases for comparing the circuit models in performance were the minimum base currents to the switching transistors (e.g., Q1 and Q2 in Figure 1) in the push-pull amplifier stage and the maximum power dissipation of the flip-flops providing the base currents. For circuit life, the comparisons are made on the basis of success probabilities or likelihoods of survival using both two-state (success vs. failure) logic and three-state (short, open, normal) logic for circuit components.

The results of performance analyses are summarized for comparison in Table III. The minimum required base currents for saturating the switching transistors during their required ON period were estimated in Section 3.1 from maximum collector current requirements and minimum values of transistor dc gain. The minimum base currents for each model are associated with Condition 1 in Table III, and the maximum power dissipation with Condition 2. Condition 1 represents a worst-case situation in which the supply voltage to the flip-flops is a minimum, the output impedance of the flip-flops is at a maximum, and the p-n voltage drops in the circuit are at their extreme value which minimizes the base current. Condition 2 represents a worst-case situation in which the supply voltage to the flip-flops is a maximum, the output impedance of the flip-flops is at a maximum, and the p-n voltage drops in the circuit are at their extreme value which maximizes the flip-flop output current and power dissipation. Resistor variations were neglected since the effect of their $\pm 1\%$ variations was determined to be insignificant.

Table III. Summary of Results of Performance Analyses

Circuit	Performance Characteristic	Model 1		Model 2		Model 3		
		Condition		Condition		Normal Operation	With Flip-flop Failure	
		1	2	1	2	Condition 1	Condition 2	Condition 1 2
Basic Timing Channel Circuit	Q1, Q2 Base Current(ma) (Min. Required 2.2 ma)	2.1	6.3	2.7	5.4	3.7	5.8	2.2 5.1
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 25°C)	12.8	28.6	14.4	25.0	17.7	26.7	17.7 26.7
Timing Channel Circuit No. 5	Q9, Q10 Base Current(ma) (Min. Required: 2.2 ma)	1.7	5.6	2.5	5.2	4.1	6.3	2.2 5.3
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 25°C)	15.7	33.2	18.0	31.6	23.4	36.4	23.4 36.4
Magnetic Amplifier Driver Circuit	Q17, Q18 Base Current(ma) (Min. Required: 2.9 ma)	---	---	4.7	8.4	5.2	7.6	3.0 6.5
	Flip-flop Power Dissipation (mw) (Rated: 50 mw at 250°C)	---	---	20.0	38.8	22.3	34.4	22.3 34.4

With reference to Table III, attention is first directed to Model 1, Condition 1 where the worst-case base currents are concluded to be inadequate. This result, coupled with considerations for life, provided the initial motivation for the investigation of possible design modifications. The maximum flip-flop power dissipation for Model 1, tabulated under Condition 2, is well within the rated capability of 50 mw for 25°C ambient temperature operation.

In redesigning to provide the minimum required base current, increased power dissipation of the flip-flops becomes a consideration. No derating recommendations for the integrated circuit flip-flop are provided by the manufacturer, therefore, no derated value was employed as a specific design criterion. The maximum flip-flop power dissipation computed for any condition is 38.8 mw, and occurs for the original version of the magnetic amplifier driver circuit, i.e., Model 2. Consequently, it is concluded that this level of flip-flop power dissipation, as estimated by the methods herein, is acceptable.

Before completing the discussion of performance comparison, the comparison of circuit life for the three models is considered. Comparisons were made on the basis of circuit success probabilities and are summarized in Table IV. Both two- and three-state logic were employed because of research interest in various analysis techniques. It is noted that the results for the two techniques are contradictory, however, more confidence is placed in the result using three-state logic because of the added depth in considering the effect of specific modes of component failure.

On the basis of three-state logic, Model 3 is the superior circuit. Model 2 does not offer improvement over Model 1 because the shorted mode of failure for the diodes on the output of the inactive flip-flop is critical. Model 3, using resistors in the coupling circuit, is specifically designed to eliminate the criticality of this type of failure. In fact, a resistor short is shown in Section 3.1 to degrade the performance less than the failure mode when the output lead of the inactive flip-flop becomes grounded. As shown in Table III for Model 3

Table IV. Summary of Results of Analyses for Circuit Life

Type Analysis	Model 1	Model 2	Model 3
Two-State Logic (Failed vs. non-failed)	P_1	$P_2 > P_1$ $P_2 = \frac{P_1}{P_{CR}^4 (2 - P_{CR})^4}$	$P_3 < P_2 \text{ and } P_3 < P_1$ $P_3 = \frac{\frac{P_1^2}{P_{R1}^2}}{P_{CR}^4 (2 - P_{CR})^4} = \frac{\frac{P_{R1}^2 P_1}{P_{CR}^4 (2 - P_{CR})^8}}{P_{CR}^4 (2 - P_{CR})^4}$
Three-State Logic (Short, open, normal)	P'_1	$P'_2 < P'_1$ $P'_2 = \frac{P'_1}{P_o^2 (2 - P_o)^2 (2 - P_s)^2}$	$P'_3 > P'_2 \text{ and } P'_3 > P'_1$ $P'_3 = \frac{\frac{P'_1}{P_o^2 (2 - P_o)^2 P_s}}{P_o^2 (2 - P_o)^2 P_s} = \frac{P'_1}{P_o^4 (2 - P_o)^4 P_s^2 (2 - P_s)^2}$

Legend: P_j = probability of survival of model j circuit using two-state logic

P'_j = probability of survival of model j circuit using three-state logic

P_{CR} = probability of survival of diodes

P_{R1} = probability of survival of resistor R1

P_o = probability of diode not failing open

P_s = probability of diode not failing short

with this mode of flip-flop failure, the base current is 2.2 ma for the timing channel circuits; this value representing the minimum required value. Maximum power dissipation of the flip-flop for this model is noted as 36.4 mw. A similar argument is applicable to Model 3 of the magnetic amplifier driver circuit.

On the basis of two-state logic, Model 2 appears to be the best circuit, however, because this approach neglects modes of failure, there is less confidence in the results than in those obtained with three-state logic. Elimination of eight diodes in using Model 2 instead of Model 1 results in the improvement shown. The similar effect of further elimination of the remaining eight diodes by Model 3 is offset by the addition of the two resistors. Since conventional treatment with two-state logic automatically considers a failure of these added components as critical, the result differs from that obtained with three-state logic.

The above arguments point to Model 3 as the preferred circuit for use in the inverter. Model 1 is definitely ruled out.

As shown in Table III, Model 2 offers some improvement in performance over Model 3 in that additional safety margin for regulating the base currents is available and flip-flop power dissipation is less. Whether the improvement in performance more than offsets the decrease in likelihood of survival is subject to question, but the considerations of Model 2 as a candidate for use in the inverter were justified. Adequate quantitative assessment of the trade-off between performance and life in comparing Models 2 and 3 could be obtained only by constructing numerous circuits and testing them under various conditions.

In final summary, Model 3 of the timing channel circuits and the magnetic amplifier driver circuit is recommended for use in the static inverter. This recommendation is based strongly on the analysis results and arguments presented above but is supported by the engineering confidence achieved from familiarity gained with the circuit during the analysis and the observations with breadboarded versions of the circuit.

7.0 References

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